National Semiconductor

MICROCIRCUIT DATA SHEET

MNLF147-X REV 0A2

Original Creation Date: 02/08/95
Last Update Date: 11/23/98
Last Major Revision Date: 02/08/95

WIDE BANDWIDTH QUAD JFER INPUT OPERATIONAL AMPLIFIER

General Description

The LF147 is a low cost, high speed quad JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II[TM] technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF147 is pin compatible with the standard LM148. This feature allows designers to immediately upgrade the overall performance of existing LF148 and LM124 designs.

The LF147 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift.

Industry Part Number

LF147

NS Part Numbers

LF147J/883

Prime Die

LF147

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-833 , Method 5005

Subgrp	Description	Temp (^{O}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Internally trimmed offset voltage	5mV Max
- Low input bias current	50pA Typ
- Low input noise current	0.01pA/Root Hz Typ
- Wide gain bandwidth	4MHz Typ
- High slew rate	13V/uS Typ
- Low supply current	7.2mA Typ
- High input impedance	10E12 Ohms Typ
- Low total harmonic distortion Av=10, RL = 10K, Vo = 20Vp-p, BW = 20Hz - 20KHz	<0.02% Typ
- Low 1/f noise corner	50Hz Typ
- Fast settling time to 0.01%	2uS Typ

(Absolute Maximum Ratings)

Supply Voltage	±22V
Differential Input Voltage	±38V
Input Voltage Range (Note 1)	±19V
Output Short Circuit Duration (Note 2)	Continuous
Power Dissipation (Note 3, 4)	900mW
Tj Max	150 C
ThetaJa Ceramic DIP (J) Package	70 C/W
Operating Temperature Range	-55 C ≤ Ta ≤ 125 C
Storage Temperature Range	-65 C ≤ Ta ≤ 150 C
Lead Temperature (Soldering, 10 seconds)	260 C
Soldering Information Dual-In-Line Package (Soldering, 10 seconds)	260 C
ESD Tolerance (Note 5)	900V

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
Note 2: Any of the amplifier outputs can be shorted to ground indefinately, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.
Note 3: For operating at elevated temperature, these devices must be derated based on a thermal resistance of ThetaJa.
Note 4: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.
Note 5: Human body model, 1.5K Ohms in series with 100pF.

Electrical Characteristics

DC PARAMETERS:

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vs = ±20V, Vcm = 0V, RS = 50 Ohms

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input Offset Voltage	RS = 10K Ohms				5	mV	1
						8	mV	2, 3
Iio	Input Offset Current	RL = 10K Ohms				.1	nA	1
						25	nA	2, 3
Iib	Input Bias Current	RL =10K Ohms			-.2	.2	nA	1
					-50	50	nA	2, 3
Vcm	Input Common Mode Voltage Range		1		-16	16	V	1, 2, 3
CMRR	Common Mode Rejection Ratio	Rs ≤ 10K Ohms, Vcm = ±16V			80		dB	1, 2, 3
PSRR	Power Supply Rejection Ratio	Vs = ±20V to Vs = ±5V			80		dB	1, 2, 3
Is	Supply Current					11	mA	1, 2, 3
Ios	Output Short Circuit	Vs = ±15V, Vin = +1V, Output short to GND			-13	-57	mA	1, 3
		Vs = ±15V, Vin = +1V, Output short to GND			-6	-40	mA	2
		Vs = ±15V, Vin = -1V, Output short to GND			13	57	mA	1, 3
		Vs = ±15V, Vin = -1V, Output short to GND			6	40	mA	2
AVS	Large Signal Voltage Gain	Vs = ±15V, Vo = 0 to +10V, RL=2K Ohms, RS=10K Ohms	2		50		V/mV	4
		Vs = ±15V, Vo = 0 to +10V, RL=2K Ohms, RS=10K Ohms	2		25		V/mV	5, 6
		Vs = ±15V, Vo = 0 to -10V, RL=2K Ohms, RS=10K Ohms	2		50		V/mV	4
		Vs = ±15V, Vo = 0 to -10V, RL=2K Ohms, RS=10K Ohms	2		25		V/mV	5, 6
Vo	Output Voltage Swing	Vs = ±15V, RL = 10K Ohms, Vin = +1V			12		V	4, 5, 6
		Vs = ±15V, RL = 10K Ohms, Vin = -1V				-12	V	4, 5, 6
		Vs = ±15V, RL = 2K Ohms, Vin = +1V			10		V	4, 5, 6
		Vs = ±15V, RL = 2K Ohms, Vin = -1V				-10	V	4, 5, 6

Electrical Characteristics

AC PARAMETERS:

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vs = ±20V, Vcm = 0V, RS = 50 Ohms

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Sr	Slew Rate	Vin = -5V to +5V, Av=1 RL=2K Ohms, CL = 100pF			8		V/us	7
					5		V/us	8A, 8B
		Vin = +5V to -5V, Av=1 RL=2K Ohms, CL = 100pF			8		V/uS	7
					5		V/uS	8A, 8B

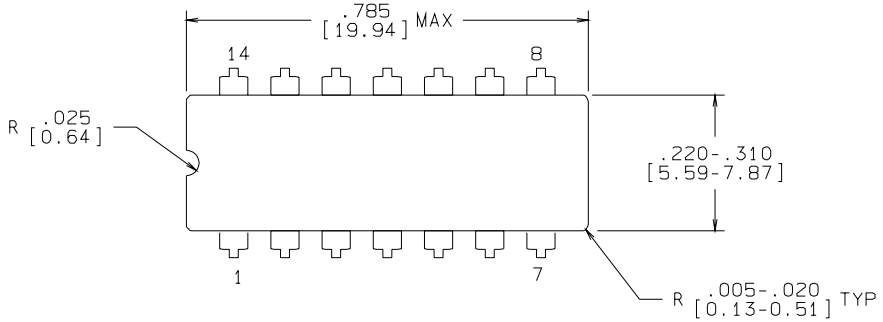
Note 1: Guaranteed by CMRR test.
Note 2: V/mV in units column is equivalent to K in datalog

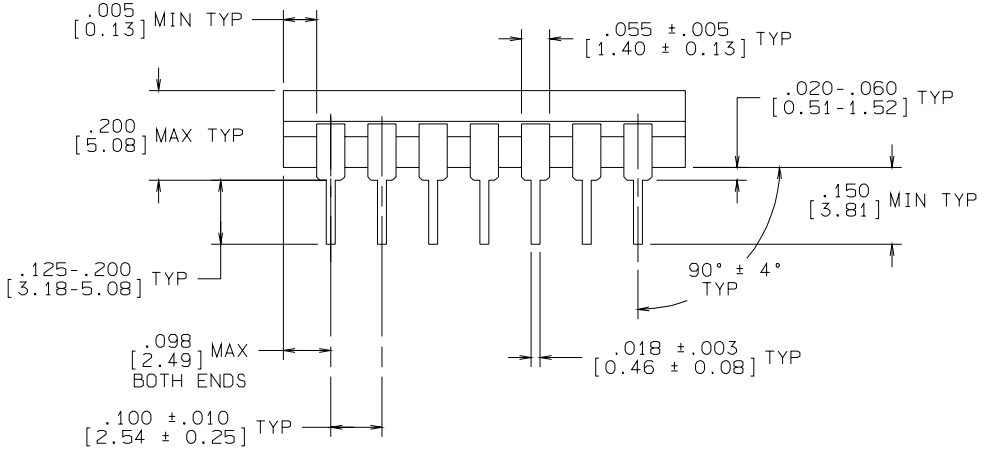
Graphics and Diagrams

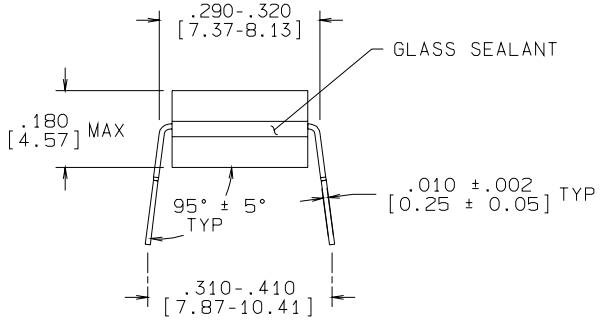
GRAPHICS#	DESCRIPTION
05486HRA3	CERDIP (J), 14 LEAD (B/I CKT)
J14ARH	CERDIP (J), 14 LEAD (P/P DWG)
P000193A	CERDIP (J), 14 LEAD (PINOUT)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
H	REVISE PER CURRENT STD; REDRAW	10001	09/15/93	TL/







CONTROLLING DIMENSION: INCH

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AB, DATED 04/1981.

APPROVALS	DATE
DRAWN T. LEQUANG	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
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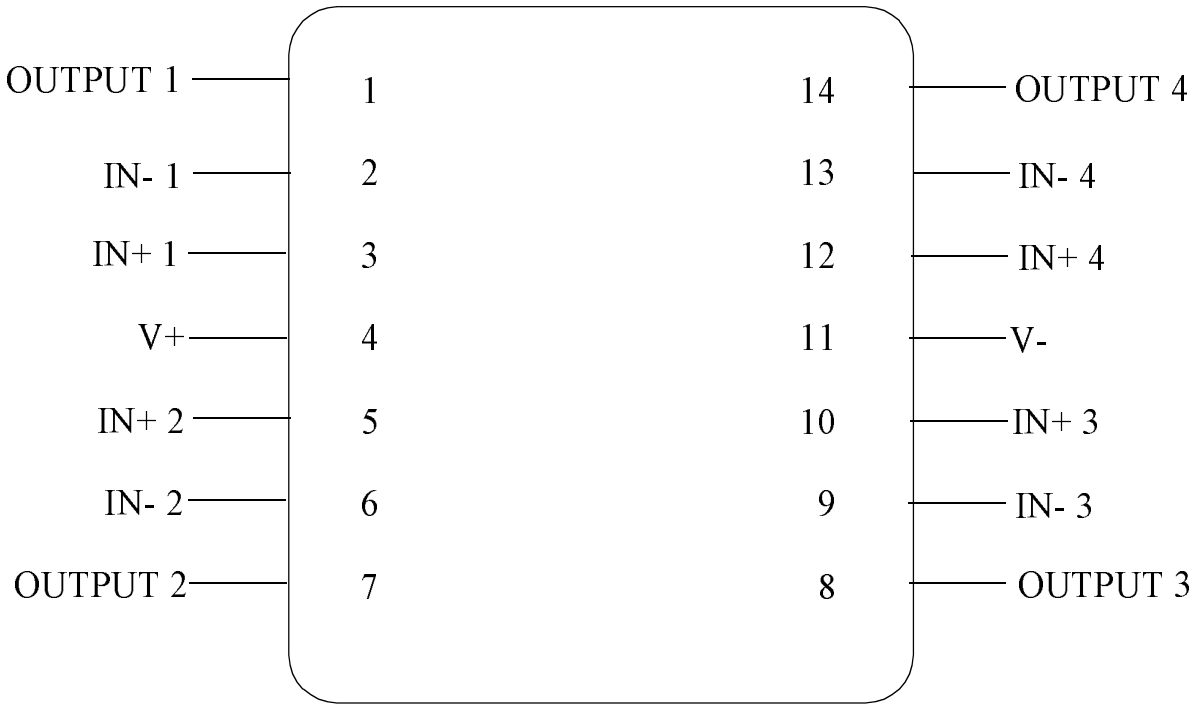
CERDIP (J), 14 LEAD,

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J14A	H

DO NOT SCALE DRAWING | SHEET 1 OF 1



LF147J
14 - LEAD DIP
CONNECTION DIAGRAM
TOP VIEW
P000193A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A1	M0002783	11/23/98	Barbara Lopez	Updated MDS: MNLF147-X Rev 0A0 to MNLF147-X Rev 0A1. Updated Burn-in Graphic and added Pinout.
0A2	M0003085	11/23/98	Rose Malone	Update MDS: MNLF147-X, Rev. 0A1 to MNLF147-X, Rev. 0A2.